

CLAIMS

1. (Previously Presented) An interconnection structure of a semiconductor device having a dummy interconnection electrically connected to an interconnection forming a portion of a circuit, said dummy interconnection provided with a stress concentration portion having tensile stress higher than that of said interconnection generated therein, and

wherein the tensile stress in said stress concentration portion is not less than 200MPa nor more than 400Mpa.

2. (Previously Presented) The interconnection structure of a semiconductor device according to claim 1, wherein said dummy interconnection has a first end portion and a second end portion, said first end portion electrically connected to said interconnection and said second end portion electrically disconnected.

3. (Original) The interconnection structure of a semiconductor device according to claim 2, wherein said dummy interconnection is formed of a via.

4. (Original) The interconnection structure of a semiconductor device according to claim 1, wherein the tensile stress is generated in said stress concentration portion by providing an insulating film having internal stress of compression, in proximity to said stress concentration portion or in contact with said stress concentration portion.

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5. (Original) The interconnection structure of a semiconductor device according to claim 4, wherein said insulating film is a SiN film deposited by plasma CVD.

Claims 6-11. (Cancelled)